Exhibit 21

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

OAKLAND DIVISION

NETLIST, INC.,

Plaintiff,

v.

GOOGLE INC.,

Defendant.

CASE NO. CV-09-05718 SBA
[Related to Case No. CV-08-04144 SBA]

JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT UNDER PATENT LOCAL RULE 4-3

Pursuant to Patent L.R. 4-3 of the Local Rules of Practice for Patent Cases before the United States District Court for the Northern District of California, Plaintiff Netlist, Inc. ("Netlist") and Defendant Google Inc. ("Google"), by and through their respective undersigned counsel, submit the following Joint Claim Construction and Prehearing Statement ("Joint Statement").

I. Construction Of Claim Terms On Which The Parties Agree (Patent L.R. 4-3(a))

The chart attached as Exhibit A to this Joint Statement lists the constructions of the claim terms and clauses of U.S. Patent No. 7,619,912 ("the '912 Patent") on which the parties agree. The agreed to constructions for the claim terms "logic element," "signal," and "control signals" were construed by the Court in related case *Google Inc. v. Netlist, Inc.*, CV-08-04144 SBA ("the '386 Patent Case"). In addition, the parties have agreed to constructions previously stipulated to from the '386 Patent Case for the claim terms "memory devices," "coupled to the printed circuit board," "rank," "command signal," and "chip-select signal." The parties have also agreed to the constructions of the claim terms and clauses "computer system," "phase-lock loop device," "mounted to the printed circuit board," and "register."

II. Proposed Construction Of The Disputed Terms (Patent L.R. 4-3(b-c))

The chart attached as Exhibit B to this Joint Statement lists the constructions of the claim terms and clauses of the '912 Patent whose constructions the parties dispute, as well as each party's proposed constructions and supporting evidence, in accordance with Patent L.R. 4-3(b).

For purposes of Patent L.R. 4-3(c), Netlist contends that the five most significant terms in dispute are (1) "bank," (2) "the at least one integrated circuit element comprising a logic element, a register, and a phase lock loop," (3) "operatively coupled/operationally coupled," (4) "spaced from," and (5) "in a direction along the first side/in a direction along the second side."

For purposes of Patent L.R. 4-3(c), Google contends that the five most significant terms in disputed are (1) "set of input control signals" / "set of input signal" / "plurality of input control signals," (2) "set of output control signals" / "set of output signals" / "plurality of output signals," (3) "at a time," (4) "bank," and (5) claim 45 (indefiniteness).

III. Length Of Time For Claim Construction Hearing (Patent L.R. 4-3(d))

The tutorial and claim construction hearing are presently scheduled for September 9, 2010 beginning at 9 a.m. Pursuant to Judge Armstrong's Patent Standing Order, the tutorial is scheduled to last approximately one to one-and-a-half hours, with each side being allotted 30-45 minutes to present a short summary and explanation of the technology at issue.

Google Proposal for the Tutorial: Due to the parties' previous tutorial to the Court on similar technology in the '386 Patent Case, Google does not believe that a live tutorial is necessary. Google proposes that, prior to the claim construction hearing, the parties submit a written tutorial to the Court.

Joint Proposal for the Claim Construction Hearing: Pursuant to the Patent Standing Order, the claim construction hearing will normally be scheduled to last no longer than three (3) hours. Due to the parties' previous tutorials to the Court on similar technology in the '386 Patent Case, the parties believe that three (3) hours would be sufficient and appropriate for the hearing.

The parties will meet and confer on an appropriate manner of presentation for the hearing and will submit a joint proposal to the Court.

IV. Witnesses To Be Called At Claim Construction Hearing (Patent L.R. 4-3(e))

The parties identify the following witnesses to be called at the claim construction hearing.

A. Witness Netlist May Call

Netlist anticipates that it may call Richard Turley as a witness at the tutorial and claim construction hearing. Mr. Turley would be expected to explain how a person of skill in the art would interpret the claim terms at issue. Mr. Turley may also testify regarding the relevant technology at issue in this case.

B. Witness Google May Call

Google does not believe any witnesses are required; nevertheless Google reserves the right to call William Hoffman as a witness at the tutorial and claim construction hearing. Mr. Hoffman would be expected to explain how a person of skill in the art would interpret the claim terms at issue. Mr. Hoffman may also testify regarding the relevant technology at issue in this case.

DATED: June 25, 2010

LEE, TRAN & LIANG, APLC

By /s/ Steven R. Hansen
Steven R. Hansen

Attorneys for Plaintiff
NETLIST, INC.

DATED: June 25, 2010

KING & SPALDING LLP

By /s/ Scott T. Weingaertner
Scott T. Weingaertner

Attorneys for Defendant
GOOGLE INC.

DECLARATION OF CONSENT

Pursuant to General Order No. 45, Section X(B) regarding signatures, I attest under penalty of perjury that concurrence in the filing of this document has been obtained from Scott T. Weingaertner, counsel for Defendant Google Inc.

DATED: June 25, 2010

LEE, TRAN & LIANG, APLC

By /s/ Steven R. Hansen
Steven R. Hansen

Attorneys for Plaintiff
NETLIST, INC.

Exhibit A to Joint Claim Construction and Prehearing Statement under Patent L.R. 4-3

EXHIBIT A, *Netlist v. Google,* Patent Local Rule 4-3(a)

logic element	"a hardware circuit that performs a predefined function on input signals from the computer system and presents the resulting signals as its output."
signal	"a varying electrical impulse that conveys information from one point to another."
control signals	"signals, including address and command signals, that regulate system operations."
memory devices	"devices in which data is stored and retrieved."
coupled to the printed circuit board	"electrically connected to the printed circuit board."
rank	"a group of memory devices enabled to receive and transmit data by a common chip-select signal."
command signal	"a signal that initiates a predetermined type of computer operation, such as read, write, refresh or precharge."
chip-select signal	"a control signal that enables the input and output of data to and/or from a memory device."
computer system	"a server or personal computer system including a set of hardware components that are related and connected and to which a memory module is connectable"
phase-lock loop device	"a device for generating a clock signal that is related to the phase of an input reference signal"
mounted to the printed circuit board	"attached to the printed circuit board"
register	"a circuit component or components that receive, buffer, and transmit signals"

Exhibit B to Joint Claim Construction and Prehearing Statement under Patent L.R. 4-3

EXHIBIT B, *Netlist v. Google,* Patent Local Rule 4-3(b)

DISPUTED CLAIM TERMS	NETLIST'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE	GOOGLE'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE (All citations are to the '912 Patent unless otherwise noted.)
bank	Proposed Construction "a group of memory cells or locations inside a memory device" Support in Specification 1:31-34: "Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module." 1:40-44: "The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits." 1:58-61: "The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits." 9:18-21: "In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank." 21:59-61: "In certain embodiments, a copy of the A_{13} address is saved by the PLD 42 for each of the internal banks (e.g., 4 internal banks) per memory device 30."	Proposed Construction "an addressable unit of memory cells" Support The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, 2000. IEEE "bank" "A contiguous section of addressable memory." 1:31-34 "Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module." 1:58-62 "The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits." 9:57-58 "Byte 17: Defines the number of banks internal to the DRAM device used in the memory module" 10:59-62 "Each memory device 31, 33 has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations."

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DISPUTED CLAIM TERMS	NETLIST'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE	GOOGLE'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE (All citations are to the '912 Patent unless otherwise noted.)
	Extrinsic Support JEDEC, *Dictionary of Terms for Solid State Technology*, JESD88 December 2009) at 14: Bank address (BA): In a RAM that has multiple banks in its architecture, the address used to select any one of the available banks. Bruce Jacob, et al., *Memory Systems: Cache, DRAM, Disk* (Elsevier, Inc. 2008) at 321. *See, e.g.*, Figure 7.8 showing a DRAM's internal bank. Deposition Transcript of William Hoffman, dated May 18, 2010 (*Google v. Netlist*, CV08-4144) at 52, 235-236 and 267-268.	
at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop	Proposed Construction "one or more integrated circuit elements, wherein a logic element, a register, and a phase-lock loop are distributed among the one or more integrated circuit elements" Specification Support 5:37-55 "While the phase-lock loop device 50, the register 60, and the logic element 40 are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock	Proposed Construction *Google contends that the plain meaning of this phrase is apparent and, therefore, no construction by the Court is required.*

EXHIBIT B, *Netlist v. Google*, Patent Local Rule 4-3(b)

DISPUTED CLAIM TERMS	NETLIST'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE	GOOGLE'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE (All citations are to the '912 Patent unless otherwise noted.)
	loop device 50, the register 60, and the logic element 40 are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device 50 and a register 60 compatible with embodiments described herein. In certain embodiments, the memory module 10 further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board 20. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits."	
set of input control signals (claim 1)	Proposed Construction *Netlist contends that the plain meaning of this phrase is apparent and, therefore, no construction by the Court is required. However, if the Court believes that construction is required, Netlist proposes the following:* "set of input control signals" is a "set of varying electrical impulse inputs that convey information for regulating system operations, including addresses and commands, from one point to another" Specification Support Figures 1A, 1B, 2A, 3A	Proposed Construction "input control signals including at least one row/column address signal, bank address signals, and at least one chip select signal, but not including a first command signal" Support Claim 1 "A memory module connectable to a computer system, the memory module comprising: a printed circuit board; a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks; a

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DISPUTED CLAIM TERMS	NETLIST'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE	GOOGLE'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE (All citations are to the '912 Patent unless otherwise noted.)
	5:14-21: "The logic element 40 receives a set of input control signals from the computer system. The set of input control signals correspond to a second number of memory devices smaller than the first number of memory devices. The logic element 40 generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices." 6:55-7:2: "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals. In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured." 11:52-57: 11:52-57: "The logic element 40 then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10."	circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register." 6:55-64 "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column

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DISPUTED CLAIM TERMS	NETLIST'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE	GOOGLE'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE (All citations are to the '912 Patent unless otherwise noted.)
		address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals." *See* Figures 1A, 1B, 2A, 2B, 3A, and 3B
set of input signals (claim 15)	Proposed Construction *Netlist contends that the plain meaning of this phrase is apparent and, therefore, no construction by the Court is required. However, if the Court believes that construction is required, Netlist proposes the following:* "set of input signals" is a "set of varying electrical impulse inputs that convey information from one point to another" Specification Support Figures 1A, 1B, 2A, 3A 5:14-21: "The logic element 40 receives a set of input control signals from the computer system. The set of input control signals correspond to a second number of memory devices smaller than the first number of memory devices. The logic element 40 generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices."	Proposed Construction "input address signals including at least one row/column address signal, bank address signals, and at least one chip select signal, but not including a command signal" Support Claim 15 "A memory module connectable to a computer system, the memory module comprising: a printed circuit board; a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks; a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR

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DISPUTED CLAIM TERMS	NETLIST'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE	GOOGLE'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE (All citations are to the '912 Patent unless otherwise noted.)
	6:55-7:2: "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals. In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured." 11:52-57: 11:52-57: "The logic element 40 then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10."	memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register." 6:55-64 "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals." *See* Figures 1A, 1B, 2A, 2B, 3A, and 3B
set of input control signals (claim 28)	<u>Proposed Construction</u> *Netlist contends that the plain meaning of this phrase is*	<u>Proposed Construction</u> "input control signals including a row/column address

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	apparent and, therefore, no construction by the Court is required. However, if the Court believes that construction is required, Netlist proposes the following: "set of input control signals" is a "set of varying electrical impulse inputs that convey information for regulating system operations, including addresses and commands, from one point to another" <u>Specification Support</u> Figures 1A, 1B, 2A, 3A 5:14-21: "The logic element 40 receives a set of input control signals from the computer system. The set of input control signals correspond to a second number of memory devices smaller than the first number of memory devices. The logic element 40 generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices." 6:55-7:2: "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals. In certain embodiments, the set of output control signals corresponds	signal, bank address signals, a chip-select signal, and an input command signal" <u>Support</u> Claim 28 "A memory module connectable to a computer system, the memory module comprising: a printed circuit board; a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks; a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output

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DISPUTED CLAIM TERMS	NETLIST'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE	GOOGLE'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE (All citations are to the '912 Patent unless otherwise noted.)
	to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured." 11:52-57: 11:52-57: "The logic element 40 then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10."	control signals to at least one DDR DRAM device of the selected at least one rank; and a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register. 6:55-64 "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals." *See* Figures 1A, 1B, 2A, 2B, 3A, and 3B
plurality of input control signals (claim 39)	Proposed Construction *Netlist contends that the plain meaning of this phrase is apparent and, therefore, no construction by the Court is required. However, if the Court believes that construction is required, Netlist proposes the following:* "plurality of input control signals" is a "plurality of varying electrical impulse inputs that convey information for regulating system operations, including addresses and commands, from one point to another" Specification Support	Proposed Construction "input control signals including row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals" Support Claim 39 "A memory module connectable to a computer system, the memory module comprising: a printed circuit board having a first side and a second side; a plurality of double-data-rate (DDR) memory devices mounted to the

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DISPUTED CLAIM TERMS	NETLIST'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE	GOOGLE'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE (All citations are to the '912 Patent unless otherwise noted.)
	Figures 1A, 1B, 2A, 3A 5:14-21: "The logic element 40 receives a set of input control signals from the computer system. The set of input control signals correspond to a second number of memory devices smaller than the first number of memory devices. The logic element 40 generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices." 6:55-7:2: "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals. In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured." 11:52-57: 11:52-57: "The logic element 40 then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory	printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank. 6:55-64 "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column

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	devices 30 of the memory module 10."	address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals." *See* Figures 1A, 1B, 2A, 2B, 3A, and 3B
set of output control signals (claim 1)	Proposed Construction *Netlist contends that the plain meaning of this phrase is apparent and, therefore, no construction by the Court is required. However, if the Court believes that construction is required, Netlist proposes the following:* "set of output control signals" is a "set of varying electrical impulse outputs that convey information for regulating system operations, including addresses and commands, from one point to another" Specification Support Figures 1A, 1B, 2A, 3A 5:14-21: "The logic element 40 receives a set of input control signals from the computer system. The set of input control signals correspond to a second number of memory devices smaller than the first number of memory devices. The logic element 40 generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first	Proposed Construction "output control signals, not including a second command signal" Support Claim 1 "A memory module connectable to a computer system, the memory module comprising: a printed circuit board; a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks; a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of

EXHIBIT B, *Netlist v. Google*, Patent Local Rule 4-3(b)

DISPUTED CLAIM TERMS	NETLIST'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE	GOOGLE'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE (All citations are to the '912 Patent unless otherwise noted.)
	number of memory devices." 6:55-7:2: "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals. In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured." 11:52-57: 11:52-57: "The logic element 40 then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10."	DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register." 6:55-64 "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals." *See* Figures 1A, 1B, 2A, 2B, 3A, and 3B

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DISPUTED CLAIM TERMS	NETLIST'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE	GOOGLE'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE (All citations are to the '912 Patent unless otherwise noted.)
set of output signals (claim 15)	Proposed Construction *Netlist contends that the plain meaning of this phrase is apparent and, therefore, no construction by the Court is required. However, if the Court believes that construction is required, Netlist proposes the following:* "set of output signals" is a "set of varying electrical impulse outputs that convey information from one point to another" Specification Support Figures 1A, 1B, 2A, 3A 5:14-21: "The logic element 40 receives a set of input control signals from the computer system. The set of input control signals correspond to a second number of memory devices smaller than the first number of memory devices. The logic element 40 generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices." 6:55-7:2: "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes	Proposed Construction "output address signals, not including a command signal" Support Claim 15 "A memory module connectable to a computer system, the memory module comprising: a printed circuit board; a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks; a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first

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	address signals and command signals. In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured." 11:52-57: 11:52-57: "The logic element 40 then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10."	number of ranks; and a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register." 6:55-64 "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals." *See* Figures 1A, 1B, 2A, 2B, 3A, and 3B
set of output control signals (claim 28)	<u>Proposed Construction</u> *Netlist contends that the plain meaning of this phrase is apparent and, therefore, no construction by the Court is required. However, if the Court believes that construction is required, Netlist proposes the following:* "set of output control signals" is a "set of varying electrical impulse outputs that convey information for regulating system operations, including addresses and commands, from one point to another" <u>Specification Support</u>	<u>Proposed Construction</u> "output control signals including an output command signal" <u>Support</u> Claim 28 "A memory module connectable to a computer system, the memory module comprising: a printed circuit board; a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks; a circuit coupled to the printed circuit

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	Figures 1A, 1B, 2A, 3A 5:14-21: "The logic element 40 receives a set of input control signals from the computer system. The set of input control signals correspond to a second number of memory devices smaller than the first number of memory devices. The logic element 40 generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices." 6:55-7:2: "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals. In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured." 11:52-57: 11:52-57: "The logic element 40 then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory	board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register. 6:55-64 "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set

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	devices 30 of the memory module 10."	of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals." *See* Figures 1A, 1B, 2A, 2B, 3A, and 3B
plurality of output signals (claim 39)	Proposed Construction *Netlist contends that the plain meaning of this phrase is apparent and, therefore, no construction by the Court is required. However, if the Court believes that construction is required, Netlist proposes the following:* "plurality of output control signals" is a "plurality of varying electrical impulse outputs that convey information from one point to another" Specification Support Figures 1A, 1B, 2A, 3A 5:14-21: "The logic element 40 receives a set of input control signals from the computer system. The set of input control signals correspond to a second number of memory devices smaller than the first number of memory devices. The logic element 40 generates a set of output control signals in response to the set of input control signals. The set of output control signals corresponds to the first number of memory devices." 6:55-7:2: "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address	Proposed Construction "output control signals including row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals" Support Claim 39 "A memory module connectable to a computer system, the memory module comprising: a printed circuit board having a first side and a second side; a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals; and at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element comprising a logic element, a register, and a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a

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	signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals. In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured." 11:52-57: 11:52-57: "The logic element 40 then receives a set of input control signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output control signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10."	second number of chip-select signals less than the first number of chip-select signals, wherein the logic element receives the bank address signals and at least one command signal of the plurality of input signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank. 6:55-64 "As schematically illustrated by FIGS. 1A and 1B, in certain embodiments, the logic element 40 receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) and command signals (e.g., refresh, precharge) from the computer system. In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals." *See* Figures 1A, 1B, 2A, 2B, 3A, and 3B
operatively coupled / operationally coupled	<u>Proposed Construction</u> "functionally cooperating with"	<u>Proposed Construction</u> "directly or indirectly electrically connected to provide for operation signaling"

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	Specification Support 5:28-31: "In response to signals received from the computer system, the phase-lock loop device transmits clock signals to the plurality of memory devices 30, the logic element 40, and the register 60." Extrinsic Support *Innova /Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1118 (Fed. Cir. 2004) ("'[Operatively connected]' is a general descriptive frequently used in patent drafting to reflect a functional relationship between claimed components"); *Manual of Patent Examining Procedure* (8th ed., Rev. July 2008) at § 2173.05(g). The New Oxford American Dictionary, 1193 (2nd Ed., 2005) (see Exh. B, "operative") Operative: adj. (definition 1). 1. functioning; having effect: *the transmitter is operative* | *the mining ban would remain operative.*	Support 5:22-45 "In certain embodiments, as schematically illustrated in FIG. 1A, the memory module 10 further comprises a phase-lock loop device 50 coupled to the printed circuit board 20 and a register 60 coupled to the printed circuit board 20. In certain embodiments, the phase-lock loop device 50 and the register 60 are each mounted on the printed circuit board 20. In response to signals received from the computer system, the phase-lock loop device 50 transmits clock signals to the plurality of memory devices 30, the logic element 40, and the register 60. The register 60 receives and buffers a plurality of control signals, including address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices 30. In certain embodiments, the register 60 comprises a plurality of register devices. While the phase-lock loop device 50, the register 60, and the logic element 40 are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop device 50, the register 60, and the logic element 40 are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device 50 and a register 60 compatible with embodiments described herein." *See* Figures 1A and 1B

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DISPUTED CLAIM TERMS	NETLIST'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE	GOOGLE'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE (All citations are to the '912 Patent unless otherwise noted.)
Claim 45	*Netlist contends that the plain meaning of this claim is apparent and, therefore, no construction by the Court is required. Netlist contends that claim 45 is not indefinite and fully complies with the requirements of 35 U.S.C. 112, second paragraph. As stated above, claim 39 is not limited to the inclusion of a register, phase lock loop, and logic element within a single component. Thus, claim 45 adds further limitations to those recited in claim 39.* <u>Support in Specification</u> 5:40-42: "[I]n certain other embodiments, two or more of the phase-lock loop device 50, the register 60, and the logic element 40 are portions of a single component."	*Indefinite*: Claim 45 is indefinite because it can't be construed in view of claim 39, which requires that all three functional parts be included with a single integrated circuit. As a result, claim 45 is indefinite because it tries to remove one functional part ("wherein two or more…") or claims nothing further than what is claimed in claim 39. <u>Support</u> 5:37-55 "While the phase-lock loop device 50, the register 60, and the logic element 40 are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop device 50, the register 60, and the logic element 40 are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device 50 and a register 60 compatible with embodiments described herein. In certain embodiments, the memory module 10 further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board 20. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits."

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DISPUTED CLAIM TERMS	**NETLIST'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE**	**GOOGLE'S PROPOSED CONSTRUCTIONS AND SUPPORTING EVIDENCE** (All citations are to the '912 Patent unless otherwise noted.)
spaced from	Proposed Construction *Netlist contends that the plain meaning of this phrase is apparent and, therefore, no construction by the Court is required. However, if the Court believes that construction is required, Netlist proposes:* "positioned at a distance from" Specification Support Figures 1A-B, 2A, 3A 6:64-7:19: "In certain embodiments, the set of output control signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input control signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by FIG. 1A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of FIG. 1B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module 10 actually has the first number of ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of ranks of memory devices 30. In certain embodiments, the memory module 10 simulates a virtual memory module	*Indefinite*: The specification provides no instruction regarding what "spaced from" means; there is no specificity as to the spacing required Support Although Figures 11A and 11B visually illustrate the DDR memory modules on the printed circuit board, the figures are not drawn to scale. Therefore, there is no support or definition provided for the spacing required.

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	when the number of memory devices 30 of the memory module 10 is larger than the number of memory devices 30 per memory module for which the computer system is configured to utilize." 19:53-58: "FIG. 2A schematically illustrates an exemplary memory module 10 which doubles the rank density in accordance with certain embodiments described herein. The memory module 10 has a first memory capacity. The memory module 10 comprises a plurality of substantially identical memory devices 30 configured as a first rank 32 and a second rank 34." 22:62-63: "ranks 32, 34, 36, and 38 of memory devices 30." 23:15: "the four ranks 32, 34, 36, 38 is active." 23:25: "four ranks 32, 34, 36, 38." <u>Extrinsic Support</u> The New Oxford American Dictionary, 1624 (2nd Ed., 2005) (see Exh. B, "space") Space: v. (definition 1). 1. [trans.] (usu. **be spaced**) position (two or more items) at a distance from one another: *the houses are spaced out.*	
in a direction along the first side/in a direction along the second side	<u>Proposed Construction</u> *Netlist contends that the plain meaning of this phrase is apparent and, therefore, no construction by the Court is*	*Indefinite*: The specification provides no instruction regarding the placement of ranks "in a direction"

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	required. Moreover, Netlist disagrees with Google's implicit assertion that claim 11 requires placement of ranks in a direction. Support in Specification FIGS. 11A and 11B 28:28-32: "FIGS. 11A and 11B schematically illustrate a first side 362 and a second side 364, respectively, of such a memory module 300 with eighteen 64 Mx4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) 360."	Support Although Figures 11A and 11B visually illustrate the DDR memory modules on the printed circuit board, they are not drawn to scale. Therefore, there is no support or definition provided for the placement of ranks "in a direction." 28:28-32 "11A and 11B schematically illustrate a first side 362 and a second side 364, respectively, of such a memory module 300 with eighteen 64 Mx4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) 360." *See* Figures 11A and 11B
at a time	Proposed Construction *Netlist contends that the plain meaning of this phrase is apparent and, therefore, no construction by the Court is required.* Support in Specification Table 1 (Column 8) 8:44-63: "The 'Command' column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g.,	Proposed Construction "at the same time" Support Claim 18 "The memory module of claim 15, wherein the command signal is transmitted to two ranks of the first number of ranks at a time." 8:44-64 "The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is

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	read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently."	sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently. *See* Figures 1A and 1B *See* Tables 1 and 2